

E: Remarks:

The amendment filed 26 July 2004 was prepared to comply with and be in accordance with the latest instructions on preparing amendments issued by the U.S. Patent And Trademark Office dated 1/31/03 which waives the provisions of 37 CFR 1.121(a), (b), (c) and (d). It is corrected herewith as noted by the Examiner in his Notice of Non-Compliant Amendment dated 8/20/2004. Entry is now requested of this corrected amendment.

The amendment is believed to be in accordance with the examiner's suggestions. The claims 15, 16 and 17 remain, with limitations of claim 4 and 14 included in Claim 15.

The examiner is thanked for his careful reading of the description. A substitute specification and drawings are submitted as discussed 4/20/2004 with the Examiner. No new matter has been included.

Before describing the changes to the description submitted as a substitute, the undersigned would like to point out that the original description as to the subject matter claimed was complete and correct. However, there were numbers used which were derived from other applications incorporated by reference, and those have been corrected here.

As to Figure 7, the picture is actually correct, but the explanation is a little involved. The difference is mainly because each L2 cache line can contain either 64B worth of data or 32B worth of instruction (that is 8 instructions, each 4B). If the line contains instruction (type bit = I), then using 32B allows room for keeping the "Hint Instructions".

I-line: If the line contains instructions, then it only has 32B worth of instructions. So to index the cache, we need 43:58 bits (drop the last 5-bits for 32B in each line). Bits 43:58 are 16 bits, and we need a total of 16-bits to index 0 through 65535



entries. The "Address of the first instruction" needs to be 0:42 bits. This is because, we drop the last 5-bits (from 0:63) since 32B in each line and we drop the next 16-bits to index 0 through 65535 entries. So, we only need to compare 0:42 bits from the directory for a hit.

D-line: If the line contains data, then it has 64B worth of data. Since it is double that of instruction, everything gets shifted to left by 1.

Accordingly, no change is necessary in the addressing used throughout the Figures as they are correct.

In the substitute specification, the following changes were generally made. The docket number of the referenced application became U.S. Patent 6598152 on July 22, 2003. That has been changed through.

Element 206 is shown on page 20, line 22, and page 30, line 23. Element 203 is on page 13, line 25 for Figure 2 and for page 16 line 1 for Figure 3. Element 311 was changed to 207 in Figure 3, as it is the element described as 207 instead of 311 on page 33 in this specification as shown in the drawing. 204 is shown in Figures 2, and 3 and described in page 10, line 12 and 13 and Page 16 line 2 for the BHT Table. The Figure 1 has been changed to Id_bht op for identifying the op loaded into the field throughout, so the operation load was correct for the Id_bht load operation for page 12, line 10, but the quotation mark was moved to make this clear. The element 211 was used twice because of the referenced application used that number for the branch execution unit with sequencing logic which here should be and is numbered 217A and 209, etc. The text in the second paragraph has been corrected to reference 209, 216, 217A in lieu of 214 and 211.



Page 36 has been correct to change Branch execution logic to 217A with outputs 316A and 316B.

These changes have been made thoughtout the description. No new matter has been introduced. The other changes suggested by the examiner in the action have been adopted.

It is respectfully submitted that the application should be in final condition for allowance which is respectfully requested.

RESPECTFULLY SUBMITTED

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